ABSTRACT

A pull-up transistor array for a high voltage output circuit is provided. The transistor array includes a semiconductor substrate, an epitaxial layer formed on the semiconductor substrate and N double diffused MOS transistors (DMOS transistors) laterally arranged on the epitaxial layer. One of source/drains of the DMOS transistors is formed at each of transistors, and the N DMOS transistors share another source/drain. Accordingly, the pull-up transistor array may output a signal of a high voltage and high current, and may high-integrate a device because a device isolation region is not required between the DMOS transistors.